4-6-04

Image AF/2833$

DOCKET NO.: FCI-2462/C2346 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Donald K. Harper

Application No.: 09/460,007

Filing Date: December 13, 1999

Confirmation No.: 1903

Group Art Unit: 2833

Examiner: Truc T. Nguyen

For: ELECTRICAL CONNECTOR HOUSING

EXPRESS MAIL LABEL NO: EL999292200US
DATE OF DEPOSIT: April 5, 2004

EL999292200US

MS Appeal Brief - Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF TRANSMITTAL
PURSUANT TO 37 CFR § 1.192

Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal received by The United States Patent and Trademark Office on **March 11, 2004.**

☐ Applicant(s) has previously claimed small entity status under 37 CFR § 1.27 .

☐ Applicant(s) by its/their undersigned attorney, claims small entity status under 37 CFR § 1.27 as:

- ☐ an Independent Inventor
- ☐ a Small Business Concern
- ☐ a Nonprofit Organization.

☐ Petition is hereby made under 37 CFR § 1.136(a) (fees: 37 CFR § 1.17(a)(1)-(4) to extend the time for response to the Office Action of to and through comprising an extension of the shortened statutory period of month(s).

	SMALL ENTITY		NOT SMALL ENTITY	
	RATE	FEE	RATE	FEE
☒ APPEAL BRIEF FEE	$165	$	$330	$330.00
☐ ONE MONTH EXTENSION OF TIME	$55	$	$110	$
☐ TWO MONTH EXTENSION OF TIME	$210	$	$420	$
☐ THREE MONTH EXTENSION OF TIME	$475	$	$950	$
☐ FOUR MONTH EXTENSION OF TIME	$740	$	$1480	$
☐ FIVE MONTH EXTENSION OF TIME	$1005	$	$2010	$
☐ LESS ANY EXTENSION FEE ALREADY PAID	minus	($)	minus	($)
TOTAL FEE DUE		$0		$330.00

☒ The Commissioner is hereby requested to grant an extension of time for the appropriate length of time, should one be necessary, in connection with this filing or any future filing submitted to the U.S. Patent and Trademark Office in the above-identified application during the pendency of this application. The Commissioner is further authorized to charge any fees related to any such extension of time to Deposit Account 23-3050. This sheet is provided in duplicate.

☒ A check in the amount of **$330.00** is attached. Please charge any deficiency or credit any overpayment to Deposit Account No. 23-3050.

☐ Please charge Deposit Account No. 23-3050 in the amount of **$ .00**. This sheet is attached in duplicate.

☒ The Commissioner is hereby requested to grant an extension of time for the appropriate length of time, should one be necessary, in connection with this filing or any future filing submitted to the U.S. Patent and Trademark Office in the above-identified application during the pendency of this application. The Commissioner is further authorized to charge any fees related to any such extension of time to deposit account 23-3050. This sheet is provided in duplicate.

Date: April 5, 2004

Jonathan M. Waldman
Registration No. 40,861

Woodcock Washburn LLP
One Liberty Place - 46th Floor
Philadelphia PA 19103
Telephone: (215) 568-3100
Facsimile: (215) 568-3439

DOCKET NO.: FCI-2462/C2346 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Donald K. Harper Confirmation No.: **1903**

Serial No.: **09/460,007** Group No.: **2833**

Filed: **December 13, 1999** Examiner: **Truc T. Nguyen**

For: **ELECTRICAL CONNECTOR HOUSING**

EXPRESS MAIL LABEL NO: EL999292200US
DATE OF DEPOSIT: April 5, 2004

MS Appeal Brief – Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPELLANT'S BRIEF UNDER 37 C.F.R. § 1.192

This brief is in support of Appellant's appeal from the rejection of claims 22-31 dated January 29, 2004. A Notice of Appeal was filed on March 11, 2004.

A. REAL PARTY IN INTEREST

The inventor in the present application has assigned his interest to FCI AMERICAS TECHNOLOGY INC., f/k/a BERG TECHNOLOGY, INC. The original Assignment document, to BERG TECHNOLOGY, INC., was filed for recordation in the U.S. Patent and Trademark Office assignment system on January 14, 2000, and was recorded on January 14, 2000 at Reel 010556, Frame(s) 0342.

B. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

C. STATUS OF CLAIMS

1. Claims 22-31 are pending. Claims 22-31 are reproduced in Appendix A hereto. All claims (22-31) stand rejected under 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a), and are the subject of the present appeal.

2. Claims 22-26 and 28-31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,788,510 to Walker.

3. Claim 27 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Walker.

D. STATUS OF AMENDMENTS

No Amendments have been filed subsequent to the rejection.

E. SUMMARY OF THE INVENTION

As generally described in the "Background of the Invention", ball grid array (BGA) technology can be used to attach an integrated circuit (IC) or an electrical connector to a substrate. In general, spherical solder balls are attached to a mounting interface of the IC or electrical connector and to electrical contact pads positioned on the substrate. The IC (or electrical connector), substrate, solder balls, and electrical contact pads are then heated to a temperature at which each solder ball melts and fuses to a corresponding one of the electrical contacts pads, thereby connecting the IC or electrical connector to the substrate. BGA is also referred to as surface mount, because it eliminates the need for drilling pin receiving holes in a substrate. Electrical components are attached to a surface of the substrate, which eliminates the need for hundreds of separate pin receiving holes.

It is important that the IC or electrical connector retain a substantially flat mounting interface before, during, and after exposure to the heat of reflow. A mounting interface is defined as the surface that receives the solder balls and faces the substrate. Any warpage of the IC or electrical connector mounting interface or the substrate can cause poor soldering performance when the IC or electrical connector is reflowed onto a printed circuit board.

BGA or surface mounted electrical connectors pose a larger reflow problem than ICs because electrical connectors can have housings defined by relatively complex shapes (versus the

thin, constant, flat shape of an IC). Residual stresses in such housings can result from the molding process, from the buildup of stress as a result of contact insertion, or a combination of both. These housings may become warped or twisted either initially from the molding process or upon heating to temperatures necessary for subsequent processing, such as temperatures necessary to reflow the solder balls. Such warping or twisting of the connector housing can cause a mismatch between the connector assembly and the substrate, resulting in non-co-planarity and unreliable soldering.

The present invention is directed to a connector that exhibits high co-planarity along the mounting interface. Co-planarity of the surface mounting interface of the connector is maintained by providing an insulative connector housing in which stress buildup (and thus warpage and deformation) is avoided. The present invention accommodates the deformation or warpage caused by thermal cycling that would otherwise cause the stress buildup during a reflow process employing heat. The connector avoids stress buildup by providing a connector housing that incorporates compliant sections corresponding to the areas where the greatest deformation in the connector is expected. The connector housing has portions of housing removed at the areas where the stress buildup is expected. According to this aspect of the invention, the housing has notches or slots at locations furthest from the neutral point of the connector. By means of this arrangement, stress buildup is avoided during a reflow process employing heat, so as to minimize warping and twisting of the housing.

Fig. 3 is a side view of an exemplary BGA interface connector in accordance with the present invention, Fig. 4 is a perspective view of the BGA interface connector of Fig. 3, and Fig. 5 is a bottom perspective view of the BGA interface connector of Fig. 3. The housing 15 has openings 12 in sidewalls that are placed at desired locations so as to allow the housing 15 to be compliant along desired axes. As a result, a reduction in solder joint stress between the connector 10 and its mounting substrate (such as an underlying PWB) results. Thus, during thermal cycling, the effects of the differential in the coefficient of thermal expansion of the PWB substrate and the connector 10 are minimized. Moreover, the co-planarity of the contacts is improved, and stress buildup is avoided during a reflow process employing heat.

F. ISSUES

1. Whether claims 22-31 patentably define over U.S. Patent No. 5,788,510 to Walker.

G. GROUPING OF CLAIMS

Claims 22-31 stand or fall together.

H. ARGUMENT

Claims 22-26 and 28-31 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,788,510 to Walker. Claim 27 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Walker.

Concerning independent claims 22 and 28, in the rejection, the Examiner states that:

> Walker discloses an electrical connector (20), comprising: a dielectric housing (30) including a peripheral wall surrounding a rising above an array of contact receiving passageways (56) and having a perimeter edge (32);... area of reduced rigidity (E1) in portion of the peripheral wall (see Figure 1).
>
> Walker silently [sic] about the reduced rigidity area at which stress is built up is for preventing warpage problem of the housing. However, this feature is seen to be an inherent teaching of that device since a means of the removed portion of the peripheral wall is disclosed, and it is apparent that some type of warpage prevention must be presented in order for the device to function as intended.

Rejection of January 29, 2004, at page 2.

This rejection should be reversed for various reasons.

1. The areas of reduced rigidity in Walker do not inherently avoid stress buildup

The Examiner relies on Walker's E1 area as the sole basis of the novelty and obviousness rejections. In particular, the Examiner relies on suspect inherent teachings of Walker.

MPEP § 2131.01 (III) states:

> [t]o serve as an anticipation when the reference is silent about the asserted inherent characteristic, such a gap in the reference may be filled with recourse to extrinsic evidence. Such evidence **must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.** *Citing* Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991) (emphasis added).

The only evidence on the record is the Examiner's conclusion that Walker's E1 area inherently teaches the Applicant's claimed feature. This is a flawed statement. There is absolutely nothing in Walker to support that conclusion, and the Examiner has not offered any extrinsic evidence to support the claim rejections. Area E1 can equally be a manifestation of the manufacturing of the part, i.e., positioning tool placement.

On the other hand, Applicant claims a specific location for their area of reduced rigidity. In claim 22, for example, the areas of reduced rigidity are located where it is known that stress will build up due to the heat of the reflow process and the materials from which the connector housing is made.

The Applicant believes that the Examiner is making a good faith argument against patentability. However, good faith does not defeat the patentability of the claimed invention. Without "clear" evidence to fill the inherency "gap" in Walker, the Examiner's position is an individual opinion that does not carry any weight. Therefore, the instant claims are not anticipated or suggested by Walker.

2. Walker is in no way related to BGA technology or its problems

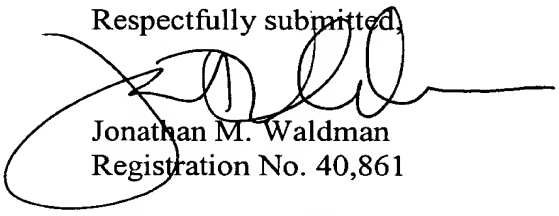
Walker discloses a through-hole connector, not a BGA type of surface mounted connector. The Walker electrical connector has pins that are forced into pre-drilled through holes defined by the substrate. The ends of the pins, which protrude through an opposed side of the substrate, are then soldered. There are no solder balls in Walker, and the entire assembly

(substrate, Walker connector, etc.) is not exposed to the same heated temperature. Co-planarity is not critical in the Walker connector because of the larger electrical contact surfaces of solder tails. Moreover, even if Walker's housing was subject to warping, the warping effect would probably have no effect on electrical connectivity between the solder tails and the substrate because the long solder tails can take up the slack of dimensional imperfections. The position of the Applicant is that no one skilled in the art would even guess that Walker's E1 area addresses a warpage problem because there would be no electrical evidence of a warpage problem in the first place. Therefore, the claimed invention is not taught or suggested by Walker.

I. CONCLUSION

For the foregoing reasons, Appellant submits that the inventions recited in claims 22-31 fully comply with the requirements of 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a). Appellant therefore requests that this patent application be remanded to the Examiner with an instruction to both withdraw the rejections for alleged unpatentability and allow the appealed claims.

Respectfully submitted,



Jonathan M. Waldman
Registration No. 40,861

Date: April 5, 2004

WOODCOCK WASHBURN LLP
One Liberty Place - 46th Floor
Philadelphia, PA 19103
(215) 568-3100

APPENDIX A

Claims on Appeal

22. An electrical connector, comprising:

a housing including a peripheral wall surrounding and rising above an array of contact receiving passageways and having a perimeter edge;

a plurality of separate surface mount contacts for connecting said housing to a substrate by a reflow process employing heat; and

areas of reduced rigidity in portions of said peripheral wall of the housing at which stress builds up due to the heat of the reflow process, each of the areas of reduced rigidity comprising portions of removed housing extending substantially perpendicular to a surface of the housing and extending through a distal end of said peripheral wall of the housing from an inner face to an outer face of the peripheral wall;

such that said areas of reduced rigidity contribute to said plurality of separate surface mount contacts better retaining their co-planarity during and after the reflow process.

23. The electrical connector according to claim 22, wherein the areas of reduced rigidity in the housing are located at positions furthest from a neutral point of the connector.

24. The electrical connector according to claim 22, wherein each of the areas of reduced rigidity comprises one of a notch and a slot.

25. The electrical connector according to claim 22, wherein the areas of reduced rigidity are disposed to absorb stress and accommodate warp.

26. The electrical connector according to claim 22, wherein the housing is made from a dielectric material.

27. The electrical connector according to claim 22, wherein the plurality of separate surface mount contacts comprise solder balls.

28. A method of reducing rigidity in a housing of an electrical connector having a plurality of separate surface mount contacts, comprising:

determining a location on said housing which may build up stress during a reflow process employing heat in which the plurality of separate surface mount contacts connect said housing to a substrate; and

removing a portion of the housing extending substantially perpendicular to a surface of the housing at said location.

29. The method according to claim 28, wherein said location is generally furthest from a neutral point of the connector.

30. The method according to claim 28, wherein said location is located to absorb stress and accommodate warp.

31. The method according to claim 28, wherein the portion is one of a slot and a notch.